CV

PERSONAL INFORMATION

Arsen Hekimyan

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arsenhekimyan@gmail.com

QUALIFICATION SUMMARY

- 5+ years of industrial experience in Analog/mixed-signal circuit design.
- Deep understanding digital/analog design concepts and methodology
- Research, design (schematic, layout), verification(DRC, LVS) and development of Low Jitter High-Speed I/O's for DDR3/LPDDR3/DDR4/LPDDR4/LPDDR4X applications for CMOS/FinFet technology processes)
- Understanding of ESD circuits design, testing (HBM, MM, CDM) and verification, whole-chip ESD protection design.
- EM & IR drop analysis on post layout design.
- High-Sigma Monte Carlo analysis on DDR I/Os.
- Experience in designing Pipeline ADC, Flash ADC, Successive Approximation ADC, LVDS, SSTL, GP and DDR I/O's libraries for CMOS/FinFET technology processes.
- Deeply understand basic circuits of analog and mixed signal circuitssuch as OpAmp, Comparator, Sense Amplifier, active filter, integrator.
- Creating project support documentation and presentation for customer
- Familiar with EDA tools: Custom Compiler, Hspice, Finesim, Cscope/WaveView, IC Compiler, Design Compiler, Milkyway,Calibre, IC Validator, Formality, VCS, Virtuoso, Spectre, NC Verilog.
- Ability to work on multiple projects simultaneously and switch quickly from one task to another
- Familiar with scripting languages: Shell, TCL

WORK EXPERIENCE

01/07/2015–Present

A&MS Circuit Design Engineer, Sr I

Synopsys Inc, Yerevan, Armenia

Research and design DDR I/Os for different protocols. Design of LPDD4/LPDDR4X/LPDDR5 –4267Mb/sto 6400Mb/s TX/RX blocks with 16nm, 14nm, 10nm, 7nm FinFet process technology.Creating reliability and Monte Carlo analysis flow for DDR I/Os. DDR I/O issue debugging and customer support.ESD protection design.

01/04/2013–31/05/2015

Researcher

National Research University of Electronic Technology, Moscow, Russia

Designing and researching low power SRAMs, high accuracy 1.5 bit/stage Pipeline ADC, Flash ADC, Successive Approximation ADC.

01/10/2013–01/03/2014

A&MS Circuit Design Engineer

Milandr, Moscow, Russia

Schematic design of DC-DC Converters, OpAmps, Comparators, Standard Cell Libraries.

01/06/2011–01/09/2012

Intern

Synopsys Inc, Yerevan, Armenia

Schematic and layout design of standard cell libraries, standard I/Os libraries, SRAM and Low power SRAM libraries. Verification standard cell libraries. Creating FRAM views. Participation on development of educational course projects and lab works. ASIC design based on Synopsys DC/ICC flow

EDUCATION

01/10/2014–present

Ph.D. student

National Research University of Electronic Technology, Moscow, Russia

01/09/2012–31/05/2014

Master's Degree, Electrical Engineering and Computer Science

National Research University of Electronic Technology, Moscow, Russia

Title of qualification awarded: Red Diploma of graduation and Certificate of Synopsys

01/09/2010–31/05/2012

Bachelor's Degree, VLSI Design

Synopsys Armenia CJSC Interdepartmental Chair

Title of qualification awarded: Red Diploma of graduation and Certificate of Synopsys

01/09/2008–31/05/2012

Bachelor's Degree, Microelectronics and semiconductor devices

State Engineering University of Armenia

LANGUAGES

- Armenian
- English
- Russian